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APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,337		08/06/2001	Shunpei Yamazaki	07977-211003	3550
26171	7590	02/25/2004		EXAMINER	
FISH & RI	CHARD	SON P.C.	NELSON, ALECIA DIANE		
1425 K STREET, N.W. 11TH FLOOR WASHINGTON, DC 20005-3500				ART UNIT	PAPER NUMBER
				2675	₽
				DATE MAILED: 02/25/2004	٥

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Advisory Action	09/924,337	YAMAZAKI ET AL.	
Advisory Action	Examiner	Art Unit	
	Alecia D. Nelson	2675	
The MAILING DATE of this communication appe	ars on the cover sheet with the o	correspondence add	ress
THE REPLY FILED 23 January 2004 FAILS TO PLACE. Therefore, further action by the applicant is required to average rejection under 37 CFR 1.113 may only be either: (1) condition for allowance; (2) a timely filed Notice of Appeal Examination (RCE) in compliance with 37 CFR 1.114.	oid abandonment of this applica a timely filed amendment whicl	ation. A proper repl h places the applica	y to a ation in
PERIOD FOR RE	PLY [check either a) or b)]		
a) The period for reply expires <u>3</u> months from the mailing date	e of the final rejection.		
b) The period for reply expires on: (1) the mailing date of this A no event, however, will the statutory period for reply expire to ONLY CHECK THIS BOX.WHEN THE FIRST REPLY WAS 706.07(f).	ater than SIX MONTHS from the mailing	g date of the final rejecti	ion.
Extensions of time may be obtained under 37 CFR 1.136(a). The fee have been filed is the date for purposes of determining the period of fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of (2) as set forth in (b) above, if checked. Any reply received by the Official filed, may reduce any earned patent term adjustment. See 37 CFR 1.136(a).	of extension and the corresponding amount the shortened statutory period for reply be later than three months after the mai	ount of the fee. The apportunity of the final originally set in the final	ropriate extension Office action; or
<ol> <li>A Notice of Appeal was filed on Appellant's 37 CFR 1.192(a), or any extension thereof (37 CFF</li> </ol>			
2. The proposed amendment(s) will not be entered be	ecause:		
(a)   they raise new issues that would require further	er consideration and/or search (	see NOTE below);	
(b) they raise the issue of new matter (see Note b	pelow);		
(c)  they are not deemed to place the application in issues for appeal; and/or	n better form for appeal by mate	rially reducing or si	mplifying the
(d) they present additional claims without canceli	ng a corresponding number of f	inally rejected claim	ıs.
NOTE: See Continuation Sheet.			
3. $\square$ Applicant's reply has overcome the following reject	tion(s):		
4. Newly proposed or amended claim(s) would canceling the non-allowable claim(s).	be allowable if submitted in a se	eparate, timely filed	amendment
5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for application in condition for allowance because:		idered but does NO	T place the
6. The affidavit or exhibit will NOT be considered bec raised by the Examiner in the final rejection.	ause it is not directed SOLELY t	to issues which wer	e newly
7. For purposes of Appeal, the proposed amendment explanation of how the new or amended claims we			and an
The status of the claim(s) is (or will be) as follows:			
Claim(s) allowed:			
Claim(s) objected to:			
Claim(s) rejected: 1-27.			
Claim(s) withdrawn from consideration:			
8. The drawing correction filed on is a) app	roved or b) disapproved by t	he Examiner.	
9. Note the attached Information Disclosure Statemen			
10. ☑ Other: <u><i>PT0</i></u> - <i>8</i> 92			,
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Ø PT0-892		2 - 20 - 20011	

## **▼** Continuation Sheet (PTOL-303)

Continuation of 2. NOTE: With regards to the request of evidence which shows that it would have been obvious for one of ordinary skill in the art at the time of the invention to allow the logic circuit to be disposed over the same substrate as the driver circuitry Shiraki et al. (U.S. Patent No. 5,844,538) teaches an active matrix image display device wherein the picture element (1), formed of a transistor (64), the scan signal line driving circuit (21), the data signal line driving circuit (22) a first frame memory (24) and a second frame memory (25) are formed on the insulating substrate (5) (see Fig. 11, column 14, lines 15-39). Therefore Shiraki et al. provides evidence for the examiner's prima facie case of obviousness.